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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/984,563	12/03/1997	JEFFREY S. MAILLOUX	95-0653.03	2304

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 03/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

HG

Office Action Summary	Application No.	Applicant(s)	
	08/984,563	MAILLOUX ET AL.	
	Examiner	Art Unit	
	Hong C Kim	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2001* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-39,59-69 and 75-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-39,59-69 and 75-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *22* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

1. Claims 36-39 and 59-69 and 70-74 are presented for examination. This office action is in response to the Amendment filed on 12/31/01.

2. Applicant amended that this application is a divisional of 08/650,719 which is CIP of 08/584,600. However, application is not entitled to the benefit of earlier filing date of 08/584,600 because claims are not supported by the parent application. It also raises 112 first paragraph issue, because 35 U.S.C. 120 states that "An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States". In other words, this application does not repeats a substantial portion of prior Application, see MPEP 201.08. Also application is not entitled to the benefit of earlier filing date of 08/584,600 because the this application is to a different inventive entity and is commonly assigned with the Patented prior application. Also it would raise an issue of double patenting since the this application is to a different inventive entity and is commonly assigned with the Patented prior application.

3. Receipt is acknowledged of information disclosure statement filed on 12/31/01, which the statement has been placed of record in the file. Information disclosed and listed on PTO 1449 was considered.

4. It is noted that this application appears to claim subject matter disclosed in the co-pending section or related section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending or related applications to avoid possible double patenting (i.e U.S Pat. No 5966724).

DOUBLE-PATENTING

5. The non-statutory double patenting rejection, whether of the obviousness-type or non-obviousness-type, is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent. *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); and *In re Goodman*, 29 USPQ2d 2010 (Fed. Cir. 1993).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(b) and (c) may be used to overcome an actual or provisional rejection based on a non-statutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.78(d).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claim 66 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 51, 59, 63, 64, and 67 of copending Application No. 08/984,561. Although the conflicting claims are not identical, they are not patentably distinct from each other because both sets of claims are related to a method of accessing a storage device, comprising: maintaining a first enabling signal in an active state, selecting burst and pipelined mode, receiving an initial external address, selecting read and write operation, cycling a second enabling signal, generating an internal address, switching the mode of operation to a pipeline mode. Both sets of claims recited similar inventive concept of accessing a memory in burst and pipelined mode except: Claim 66 of the present invention comprises less element than as claimed in the Application No. 08/984,561. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to delete additional limitation of maintaining a first enabling signal in an active state of the copending application to arrive invention of the present application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign

country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. Claims 36-39, 59-64, 69, and 75-83 are rejected under 35 USC 102(e) as being anticipated by *Manning*, U.S. Patent 5,610,864.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); choosing whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 43-54) or a pipelined mode of operation (col. 5 lines 43-50); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE).

As to claim 60, *Manning* further discloses switching between a burst mode (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipeline mode (col. 5 lines 43-50).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE).

As to claim 62, *Manning* further discloses the operations are performed in a different

order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claims 36, 75, and 80, *Manning* discloses the invention as claimed. *Manning* discloses a method for accessing an asynchronously access memory (Fig. 1 and EDO constitutes asynchrous memory, col. 6 lines 14-16), comprising the steps of: receiving an external row address to the asynchronously accessible dynamic random access memory accessible storage device (Fig. 1 and Fig. 2, ADDR, ROW); selecting or switching between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and a pipelined mode of operation (col. 5 lines 43-50); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); obtaining a first external column address (Fig. 1 and Fig. 2, ADDR, COLm).

As to claims 37, 76, and 81, *Manning* further discloses the step of obtaining a second external column address subsequent to the first external column address for operation in the pipeline mode (col. 5 lines 43-45)

As to claim 38, *Manning* further discloses generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claims 39, 77, and 82, *Manning* further discloses selecting path way (Fig. 1 Ref. 40

and col. 3 lines 20-22, col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claims 78 and 83, *Manning* further discloses switching between the pipelined mode of operation (col. 5 lines 43-50) and the burst (col. 6 lines 14-26 and col. 7 lines 43-54) and generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claim 79, *Manning* further discloses selecting at least one address pathway based on subsequently switching to the burst mode of operation (Fig. 1 Ref. 40 and col. 3 lines 20-22, col. 5 lines 43-49, col. 4 lines 23+, & col.6 lines 14+).

As to claims 63 and 69, *Manning* further discloses an external address only path for the pipeline mode (col. 5 lines 43-49, "one access per cycle" and col. 3 lines 20-22 read on this limitation); an internal buffered external address path for the burst mode of operation (col. 3 lines 20-22, col. 4 lines 23+ & col. 8 line 67); and pipeline (col. 5 lines 41-50)/burst circuitry (col. 6 lines 14-26 and col. 7 lines 43-54) .

As to claim 64, *Manning* further discloses the operations are performed in a different order (Fig. 1 Ref. 40 and col. 5 lines 43-49, col. 4 lines 23+, & col. 6 lines 14+).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 65-68 are rejected under 35 USC § 103(a) as being unpatentable over *Manning*, U.S. Patent 5,610,864 in view of *Ryan*, U.S. Patent 5,966,724 or *Rosich et al. (Rosich)*, U.S. Patent 5,587,964.

As to claim 65, *Manning* discloses a method of operating a memory circuit, comprising: receiving a mode select signal(col. 6 lines 14-34); receiving an initial external address (Fig. 1 and Fig. 2, ADDR); selecting a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); cycling a second enabling signal (Fig. 2 /CAS) ; generating an internal address (Fig. 1 Ref. 26); and receiving an external address on each cycle of the second enabling (col. 5 lines 43-49, "one access per cycle" read on this limitation). Although Manning discloses changing the mode and pipeline mode and, Manning does not specifically disclose a step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state.

Ryan discloses the step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state (Fig. 6, RAS and col. 8 lines 30-33) and receiving an external address on each cycle of the second enabling signal (Fig. 6 Ref. Addr) because it would allow the memory to switch mode of operation instantly thereby put the memory in high data throughput by eliminating the set up time (abstract lines 8-9).

One skilled in the art would have realized that maintaining a first enabling signal in active state would allow that the memory is always in ready to switch mode of operation thereby increasing the access speed of the memory.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state of Ryan in the invention of Manning because it would allow the memory to switch mode of operation thereby increasing the memory access speed. The advantage of increasing the memory speed provide sufficient suggestion and motivation to one of ordinary skill in the memory art to follow the teaching of Ryan into invention of Manning.

Alternatively, Rosich discloses the step of changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31).

One of ordinary skill in the art familiar with Manning, and looking at Rosich would have recognized that the memory access cycle of Manning would have been reduced by maintaining a first enabling signal in active state during mode of operations because it would provide capability of that the memory is always in ready to receive a mode command thereby increasing the access speed of the memory. Increasing memory speed would have a highly desirable feature in the computer system environment of Rosich because the objective of computer system is increasing speed or computing power.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the step of maintaining a first enabling signal in active state of Rosich in the invention of Manning because it would increase memory access speed of Manning by providing capability of that the memory is always in ready to receive a command. *Rosich* further discloses switching the mode select signal to select a first mode while maintaining the first enabling signal in the active state and changing the mode select signal to select a second mode (col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710).

As to claim 66, *Manning, Ryan, and Rosich* disclose the calms as the above claim 65. Manning further discloses a step of maintaining a mode select signal to select a burst mode of operation (Fig. 2 /OE, col. 7 lines 45-55 & col. 6 lines 14+) and switching the mode to a pipelined mode on successive cycles of the second enabling signal by changing the mode select signal (col. 5 lines 43-49, "one access per cycle" read on this limitation). Ryan and Rosich

discloses a step of switching the mode on the successive cycles of the second enabling signal (Fig. 6, RAS and col. 8 lines 30-33 in Ryan and col. 8 lines 24-48 and Fig. 7, Refs. 700 & 710 in Rosich).

As to claim 67, *Manning* further discloses the step of maintaining a mode select signal to select a burst mode of operation (Col. 6 lines 14-34); receiving a stream of addresses and a cycling a second enabling signal (Fig. 2 /CAS); changing the mode select signal to select a pipelined mode of operation (col. 5 lines 43-50).

As to claim 68, *Manning* further discloses the steps of selecting a pipeline mode (col. 5 lines 43-49); select an external address only path when the pipeline mode is selected (col. 5 lines 43-49, "one access per cycle" and col. 3 lines 20-22 read on this limitation); and selecting an internal buffered external address path (col. 4 lines 23+ and col. 3 lines 20-22) and generating internal column address (col. 8 line 67) when the burst mode of operation is selected.

Response to Amendment

10. Applicant's arguments filed on 12/31/01 have been fully considered but they are not persuasive.

Applicant's argument on page 3 that the reference does not disclose selecting between a burst mode and a pipeline modes of operations is not considered persuasive.

"The current invention include a pipelined architecture" (col. 5 lines 43-49 in Manning) and "switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16 & Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation, in other words, in order to work in the pipeline architecture one has to select pipeline mode. Also given the teachings of above reference one of the ordinary skill in the art at the time the invention was made would have been lead to an obvious fashion to provide a pipelined page mode circuitry since Manning discloses that the current invention include a pipelined architecture (col. 5 lines 43-49) which would increase accessing speed. Also Ryan US Patent 5,966,724 discloses additional column addresses are latched and access are performed in a pipelined page mode (col. 4 lines 22-24). Therefore, broadly written claims are disclose by the references cited.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., enabling switching between pipeline or burst operations with in the same memory, "on-the-fly") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicant's remarks on page 6 concerning references not teaching switching between the pipelined page mode and the burst mode is not considered persuasive.

"The current invention include a pipelined architecture" (col. 5 lines 43-49 in Manning) and "switching between standard fast page mode (non-EDO) and burst mode" (see col 6 lines 14-16

& Fig. 1 and col. 7 lines 44-55 in Manning) read on this limitation, in other words, in order to work in a pipelined mode one has to select that mode. Additional column addresses are latched and access are performed in a pipelined page mode (col. 4 lines 22-24 in Ryan) reads on this limitation because, in order to operate in a pipelined mode one has to select this mode.

Applicant's remarks on page 7 concerning the references not teaching changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state. Rosich discloses changing the mode select signal to select a mode of operation while maintaining a first enabling signal in an active state (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Rosich discloses a step of switching modes of operation including a step of maintaining a first enabling signal in active state (col. 8 lines 24-48 and RASL in Fig. 7, Ref. 700, page mode & 710, burst mode) for the purpose of reducing memory access time and component latency by enabling the memory chip throughout the operations (col. 1 lines 21-31).

Therefore broadly written claims are disclosed by the references cited.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3800.

16. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to TC-2100:
After-final (703) 746-7238
Official (703) 746-7239 (for formal communications intended for entry)

Non-Official/Draft (703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
March 11, 2002